IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 10/232,794
Priority Filing Date . . . . . August 28, 2002
Inventor . . . . . Luan Tran et al.
Assignee . . . . . Micron Technology, Inc.
Priority Group Art Unit 2814
Priority Examiner . . . . . H. Weiss
Attorney's Docket No. MI22-2555
Title: A Method of Forming Integrated Circuitry (As amended)

INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional application of co-pending application Serial No. 10/232,794, filed August 28, 2002, upon which the above-identified application relies for a priority date under 35 U.S.C. §120. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. §1.98(d) and MPEP §609(2). As a courtesy, copies of foreign and articles are enclosed.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: 4-21-04

D. Brent Kenady
Reg. No. 40,045

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. M122-2555	SERIAL NO. Filed Herewith
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)		APPLICANT Luan Tran et al.	
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U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,045,899	09/03/91	Arimoto			
	AB	5,107,459	04/21/92	Chu et al.			
	AC	5,350,706	09/27/94	McElroy et al.			
	AD	5,469,383	11/21/95	McElroy et al.			
	AE	5,537,347	07/16/96	Shiratake et al.			
	AF	5,508,541	04/16/96	Hieda et al.			
	AG	5,383,151	01/17/95	Onishi et al.			
	AH	5,726,092	03/10/98	Mathews et al.			
	AI	5,595,928	01/21/97	Lu et al.			
	AJ	5,747,844	05/05/98	Aoki et al.			
	AK	5,665,623	09/09/97	Liang et al.			

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AL	JP 03205868	09/09/91	Japan			Abs.	
	AM							
	AN							
	AO							
	AP							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		A. Chatterjee et al., "A Shallow Trench Isolation Study for 0.25/0.18 μm CMOS Technologies and Beyond",
			IEEE, 1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 156-57 (1996).
	AS		M. Aoki et al., "Fully Self-Aligned 6F ^{2} Cell Technology for Low Cost 1Gb DRAM", IEEE
			1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 22-23 (1996).
	AT		J.S. KIM et al., "A Triple Level Metallization Technique for Gigabit Scaled DRAMS", VMIC CONFERENCE, Technology
			Development, Memory Device Business, Samsung Electronic Co., pp. 28-33 (June 18-20, 1996).

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	AA	5,637,528	06/10/97	Higashitani et al.			
	AB	5,756,390	5/26/1998	Juengling et al.			
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	AR		B. KEETH, "A Novel Architecture for Advanced High Density Dynamic Random Access Memories",
			A Thesis for M.S. E.E., University of Idaho pp. 1-62 (i-vi); (May 1996).
	AS		T. Hamamoto et al., "NAND-Structured Trench Capacitor Cell Technologies for 256 Mb DRAM and Beyond",
			IEICE Transactions On Electronics, pp. 789-796, 1995.
	AT		M. Noguchi et al., "0.29- μm^2 Trench Cell Technologies for 1G-bit DRAMs with Open/Folded-Bit-Line Layout and Selective Growth Technique",
			1995 Symposium on VLSI Technology Digest of Technical Papers, pp. 137-138.

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	AO							
	AP							
	AQ							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		V. Mathews et al., *Dry O_2 High Presure Field Oxidation for 0.25 μm Isolation Technology*,
			SSDM '95 - Device and Process Technology, 2 pages.
	AS		Fazen, et al., "A High-C Capacitor (20.4fF/μ [2]) with Ultrthin CVD-Ta $_2O_5$ films Deposited on Rugged Poly-Si for High Density DRAMs"; 1992; 4 pps.
	AT		Fazen et al., "A Highly Manufacturable Trench Isolation Process for Deep Submicron DRAMS," ©1993 IEEE, 4 pages.

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